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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

This paper relates to several applications, listed on the attached schedule

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CHANGE OF CORRESPONDENCE ADDRESS

1. For the applications on the attached schedule, kindly update the Attorney Docket Number as indicated on the schedule.

2. Kindly change the correspondence address for these applications to:

David E. Boundy
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3. Kindly associate these applications with Customer No. 38492.

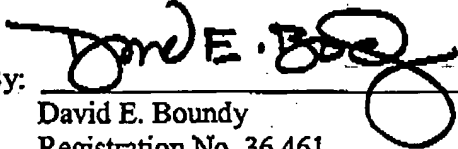
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Respectfully submitted,

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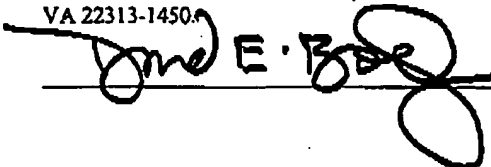
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ATTORNEY DOCKET NO.	Serial No.	Filing Date	Title
114596-03-4000	09/385,394	8/30/99	Computer For Executing Two Different Instruction Sets
114596-04-4002	09/348,317	7/7/99	Recording Classification of Instructions Executed by a Computer
114596-05-4013	09/239,194	1/28/99	Executing Programs for a First Computer Architecture on a Computer of a Second Architecture
114596-06-4003	09/322,443	5/28/99	Profiling of Computer Programs Executing in Virtual Memory Systems
114596-07-4014	09/330,852	6/11/99	Profiling Ranges of Execution of a Computer Program
114596-08-4015	09/332,263	6/11/99	Profiling Program Execution By Dense Trace Profiling and Statistical Profiling
114596-09-4016	09/425,401	10/22/99	Profiling Program Execution to Identify Frequently Executed Portions and to Assist Binary Translation
114596-10-4017	09/334,530	6/16/99	Profiling Execution of Computer Programs
114596-11-4018	09/339,749	6/24/99	Profiling Program Execution into Registers of a Computer
114596-12-4019	09/339,797	6/24/99	Modifying Program Execution Based on Profiling
114596-13-4004	09/427,168	10/26/99	Transferring Execution From One Computer Instruction Stream to Another
114596-14-4004A	09/426,989	10/26/99	Table Look-up For Control of Instruction Execution
114596-15-4004B	09/429,377	10/28/99	Improving Computer Execution by Opportunistic Adaptation
114596-16-4004C	09/429,094	10/28/99	Side Tables Annotating an Instruction Stream
114596-17-4006	09/428,850	10/28/99	Recording I/O Memory References in Program Execution Profile
114596-18-4007	09/434,198	11/4/99	Detecting Modification to Computer Memory by a DMA Device
114596-19-4008	09/432,752	11/3/99	Detecting Invalidation of Translated Object Code when Source Object Code is Modified (XP bit)
114596-20-4009	09/434,394	11/4/99	Detecting Reordered Side-Effects
114596-21-4020	09/432,753	11/3/99	Safety-Net Paradigm for Managing Two Execution Modes
114596-22-4010	09/102,028	6/22/98	Computer Modem
114596-23-4012	09/323,983	6/1/99	Reducing Modem Transmit Latency
114596-26-0051BS	09/666,110	9/20/00	Computer for Execution of Two Instruction Sets
114596-27-0052BS	09/667,226	9/21/00	Exception Mechanism for a Computer
114596-28-0053BS	09/626,325	7/26/00	Computer with Two Operating Systems
114596-29-0125BS	09/672,440	9/28/00	Managing Instruction Side-Effects
114596-30-0126BS	09/672,841	9/28/00	Validation of Memory References
114596-31-0127BS	09/672,424	9/28/00	Complex Instruction Set Computer